IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

Claims 1-20 (canceled).

21. (New) A data processor comprising;

a central processing unit (CPU) which fetches an instruction, decodes said instruction and executes said instruction;

a first data bus coupled to said CPU;

an arithmetic and logic unit which operates to perform an arithmetic operation;

a memory unit which stores results of said arithmetic operation;

a second data bus coupled to said arithmetic and logic unit and said memory unit; and

an address bus coupled to said central processing unit, said arithmetic and logic unit and said memory unit,

wherein a bit width of said second data bus is wider than a bit width of said first data bus,

wherein said CPU provides a plurality of control signals to said arithmetic and logic unit in response to a result of decoding a first instruction to control said arithmetic and logic unit, and

wherein said arithmetic and logic unit is provided data from said memory unit via said second data bus, and is capable of operating a plurality of said arithmetic

operations using said data according to said control signals related to said first instruction.

22. (New) The data processor according to claim 21, wherein said arithmetic and logic unit accesses said memory unit according to an address provided from said CPU.

23. (New) The data processor according to said claim 21, wherein said arithmetic and logic unit is provided from said data, which bit width is equal to said second data bus, according to an address from said CPU, and operates said arithmetic operations using said data.

24. (New) A data processing unit comprising:

a central processing unit (CPU) which decodes and executes instructions;

a first data bus coupled to said CPU, and having a first bit width;

a single instruction multiple data (SIMD) type arithmetic and logic unit controlled by said CPU;

a memory accessed by said SIMD type arithmetic and logic unit as a work area;

a second data bus coupled to said SIMD type arithmetic and logic unit and said memory, and having a second bit width; and

an address bus coupled to said CPU, said SIMD type arithmetic and logic unit and said memory,

wherein said second bit width is wider than said first bit width,

wherein said CPU causes said SIMD type arithmetic and logic unit to operate to perform an arithmetic operation according to a result of decoding a predetermined instruction,

wherein said CPU is capable of generating an address to access said memory by said SIMD type arithmetic and logic unit, and

wherein in accordance with a result of decoding said predetermined instruction, said SIMD type arithmetic and logic unit accesses said memory based on said address and operates a plurality of arithmetic operations using data by accessing said memory.